

CLAIMS

1. A method for testing a fixed logic device formed within a gasket, comprising:

receiving an FPGA scan chain and configuring an FPGA fabric portion for a specified test;

producing a test signal to the fixed logic device;

receiving an output test signal from the fixed logic device;

applying a signature function to the received output test signal;

repeating the producing, receiving and applying steps for a specified number of times; and

determining if a value of the signature function corresponds to an expected value.

2. The method of claim 1 further comprising the step of isolating the fixed logic device that is to be tested.

3. The method of claim 1 further comprising the step of transmitting a test signal to the fixed logic device by way of an isolation circuit element.

4. The method of claim 1 further comprising the step of receiving an output test signal from the fixed logic device by way of an isolation circuit element.

5. The method of claim 1 wherein the determining step is performed by logic within an FPGA fabric portion.

6. The method of claim 1 wherein the determining step is performed by an external tester.

7. The method of claim 1 wherein the determining step includes the step of comparing the signature to an expected value.

8. An FPGA, comprising:  
an FPGA fabric portion;  
a Gasket formed at least partially within the FPGA fabric portion, the Gasket forming interfacing logic between an embedded core device and the fabric portion; and  
isolation circuitry formed within the Gasket, the isolation circuitry being serially coupled to receive test signals from the FPGA fabric portion.

9. The FPGA of claim 8 wherein the isolation circuitry includes a multiplexer array, which multiplexer array facilitates sending test signals directly to a device under test.

10. The FPGA of claim 8 wherein the isolation circuitry includes a multiplexer array, which multiplexer array facilitates sending test signal outputs directly from a device under test to the FPGA fabric.

11. An FPGA, comprising:  
an FPGA fabric portion;  
a Gasket formed at least partially within the FPGA fabric portion, the Gasket forming interfacing logic between an embedded core device and the fabric portion;  
at least one multiplexer; and  
a fixed logic device formed within the Gasket, the fixed logic device being coupled between the multiplexer and the FPGA fabric portion.

12. The FPGA of claim 11 wherein the multiplexer is coupled to receive outputs from the fixed logic device.

13. The FPGA of claim 12 wherein the multiplexer is coupled to receive test signals from the FPGA fabric portion by way of communication paths formed within the Gasket portion, which communication paths are accessible while the FPGA is configured for testing at least a portion of the

Gasket.

14. The FPGA of claim 13 wherein the multiplexer couples the test signals received from the FPGA fabric portion to the fixed logic device whenever the FPGA is configured for testing at least a portion of the Gasket.

15. The FPGA of claim 11 wherein the multiplexer is coupled to receive outputs from an embedded core device and to produce the received outputs to the fixed logic device whenever the FPGA fabric portion is not configured to test at least a portion of the Gasket.

16. An array of isolation circuit elements formed within a Gasket surrounding an embedded fixed logic core device, all within an FPGA, comprising:

at least one isolation circuit element configured for isolating the embedded fixed logic core device; and

at least one isolation circuit element configured for isolating a fixed logic device formed within the Gasket.

17. The array of claim 16 being coupled to receive outputs from the embedded fixed logic core device and to produce the outputs to one of a fixed logic device or to a fabric portion of the FPGA.

18. The array of claim 16 being coupled to receive outputs from the fixed logic device and test signals from a fabric portion of the FPGA and to produce the received signals to an embedded fixed logic core device according to whether the FPGA is configured for performing test or for routine operations.

19. An FPGA, comprising:

ID circuitry for delivering a device ID to an embedded device;

input circuitry for receiving test signals from test

circuitry; and

multiplexer circuitry coupled to receive input test signals and control signals from the input circuitry and ID information from the ID circuitry, and to produce selected input signals to the embedded device.

20. The FPGA of claim 19 further comprising test circuitry coupled to the input circuitry to produce test and control signals thereto.

21. The FPGA of claim 19 being configurable to connect the input circuitry to pins that may be connected to external test equipment, which external test equipment is for producing test signals that are received by the multiplexer circuitry and conducted to the inputs of the embedded device.

22. An FPGA configured in a test mode of operation, comprising:

first logic circuitry forming a plurality of latches for receiving an FPGA scan chain containing test vectors;

second logic circuitry forming a test output signature generator;

third logic circuitry configured for performing a specified test; and

fourth logic circuitry for determining whether the FPGA passed or failed a test.

23. The FPGA of claim 22 wherein each of the first, second and third logic circuitry are formed to communication with a fixed logic device within an FPGA Gasket.

24. The FPGA of claim 23 wherein the fixed logic device is formed within the Gasket.

25. The FPGA of claim 23 wherein the fixed logic device is an embedded core processor that is embedded within the Gasket.

26. An FPGA, comprising:  
an FPGA fabric portion;  
a gasket forming an interfacing logic portion between an embedded device and the FPGA fabric portion;  
a first communication path in the gasket that directly couples at least one pin of the embedded device to the FPGA fabric portion; and  
a second communication path in the gasket that directly couples the FPGA fabric portion to test circuitry formed within the gasket, which test circuitry further is coupled to at least one pin of the embedded device.

27. The FPGA of claim 26 wherein the test circuitry couples the FPGA fabric portion to at least one pin of the embedded device whenever the FPGA is configured to test the embedded device.

28. The FPGA of claim 26 wherein the first communication path is for conducting at least one device scan chain to the embedded core device.

29. An FPGA, comprising:  
an FPGA fabric portion;  
a gasket forming an interfacing logic portion between an embedded device and the FPGA fabric portion;  
a first communication path in the gasket that directly couples the FPGA fabric portion to test circuitry formed within the gasket;  
a second communication path in the gasket that directly couples at least one pin of an embedded device to the test circuitry; and  
a third communication path in the gasket that couples an output of the test circuitry to an input of a fixed logic device formed within the gasket.

30. The FPGA of claim 29 wherein the test circuitry couples the FPGA fabric portion to the input of the fixed

fixed logic device.

chain to the embedded core device.

Country	Year	Population (millions)	Urban population (millions)	Urban population (%)	Population density (per sq km)	Urban population density (per sq km)
Algeria	1980	12.5	5.5	44	100	180
Algeria	1985	13.5	6.5	48	110	190
Algeria	1990	14.5	7.5	52	120	200
Algeria	1995	15.5	8.5	55	130	210
Algeria	2000	16.5	9.5	58	140	220
Algeria	2005	17.5	10.5	60	150	230
Algeria	2010	18.5	11.5	62	160	240
Algeria	2015	19.5	12.5	64	170	250
Algeria	2020	20.5	13.5	66	180	260
Algeria	2025	21.5	14.5	67	190	270
Algeria	2030	22.5	15.5	69	200	280
Algeria	2035	23.5	16.5	70	210	290
Algeria	2040	24.5	17.5	71	220	300
Algeria	2045	25.5	18.5	73	230	310
Algeria	2050	26.5	19.5	74	240	320
Algeria	2055	27.5	20.5	75	250	330
Algeria	2060	28.5	21.5	76	260	340
Algeria	2065	29.5	22.5	77	270	350
Algeria	2070	30.5	23.5	77	280	360
Algeria	2075	31.5	24.5	78	290	370
Algeria	2080	32.5	25.5	79	300	380
Algeria	2085	33.5	26.5	80	310	390
Algeria	2090	34.5	27.5	80	320	400
Algeria	2095	35.5	28.5	80	330	410
Algeria	2100	36.5	29.5	81	340	420
Algeria	2105	37.5	30.5	81	350	430
Algeria	2110	38.5	31.5	82	360	440
Algeria	2115	39.5	32.5	83	370	450
Algeria	2120	40.5	33.5	83	380	460
Algeria	2125	41.5	34.5	83	390	470
Algeria	2130	42.5	35.5	84	400	480
Algeria	2135	43.5	36.5	84	410	490
Algeria	2140	44.5	37.5	84	420	500
Algeria	2145	45.5	38.5	85	430	510
Algeria	2150	46.5	39.5	85	440	520
Algeria	2155	47.5	40.5	85	450	530
Algeria	2160	48.5	41.5	86	460	540
Algeria	2165	49.5	42.5	86	470	550
Algeria	2170	50.5	43.5	86	480	560
Algeria	2175	51.5	44.5	86	490	570
Algeria	2180	52.5	45.5	87	500	580
Algeria	2185	53.5	46.5	87	510	590
Algeria	2190	54.5	47.5	87	520	600
Algeria	2195	55.5	48.5	87	530	610
Algeria	2200	56.5	49.5	88	540	620
Algeria	2205	57.5	50.5	88	550	630
Algeria	2210	58.5	51.5	88	560	640
Algeria	2215	59.5	52.5	88	570	650
Algeria	2220	60.5	53.5	89	580	660
Algeria	2225	61.5	54.5	89	590	670
Algeria	2230	62.5	55.5	89	600	680
Algeria	2235	63.5	56.5	89	610	690
Algeria	2240	64.5	57.5	89	620	700
Algeria	2245	65.5	58.5	90	630	710
Algeria	2250	66.5	59.5	90	640	720
Algeria	2255	67.5	60.5	90		